CLAIMS

[1] An insulated gate semiconductor device (1), comprising:

a first semiconductor region (11) having a first conductivity type;

second semiconductor regions (12) having a second conductivity type, formed in one principal surface of said first semiconductor region (11);

third semiconductor regions (13) having the second conductivity type, formed in surface regions of the other principal surface of said first semiconductor region (11);

fourth semiconductor regions (14) having the first conductivity type, formed in surface regions of said third semiconductor regions (13);

a first electrode (23) electrically connected to said fourth semiconductor regions (14);

a control electrode (21) disposed, via an insulating film (22), on the other principal surface between said first semiconductor region (11) and said fourth semiconductor regions (14); and

a second electrode (20) electrically connected to said second semiconductor regions (12),

wherein said insulated gate semiconductor device comprises:

a fifth semiconductor region (15) having the first conductivity type, formed in the one principal surface of said first semiconductor region (11) so as to be adjacent to said second semiconductor regions (12); and

a sixth semiconductor region (16) having the second conductivity type, formed between said fifth semiconductor region (15) and said first semiconductor region (11).

[2] The insulated gate semiconductor device according to claim 1,

wherein said sixth semiconductor region (16) is formed between a side of said fifth semiconductor region (15) closer to the other principal surface and said first semiconductor region (11).

[3] The insulated gate semiconductor device according to claim 1,

wherein said fifth semiconductor region (15) is formed so as to be more prominent than said second semiconductor regions (12).

[4] The insulated gate semiconductor device according to claim 1,

wherein a width of said sixth semiconductor region (16) is smaller than a width of said fifth semiconductor region (15).

[5] The insulated gate semiconductor device according to claim 1,

wherein said sixth semiconductor region (16) is formed such that at least a part of said fifth semiconductor region (15) contacts said first semiconductor region (11).

[6] The insulated gate semiconductor device according to claim 1,

wherein concentration of an impurity of the second conductivity type in said sixth semiconductor region (16) is 1×10^{15} to 5×10^{18} cm^{-3}.

[7] The insulated gate semiconductor device according to claim 1,

wherein said fifth semiconductor region (15) is formed so as not to face said third semiconductor regions (13).

[8] The insulated gate semiconductor device according to claim 1,

wherein said first semiconductor region comprises a first region (11) and second regions (17) higher in impurity concentration than said first region (11), and said second regions (17) are adjacent to said fifth semiconductor region (15).

[9] A method for manufacturing an insulated gate semiconductor device comprising: a first semiconductor region (11) having a first conductivity type; second semiconductor regions (12) having a second conductivity type, formed in one principal surface of said first semiconductor region (11); third semiconductor regions (13) having the second conductivity type, formed in surface regions of the other principal surface of said first semiconductor region (11); fourth semiconductor region (14) having the first conductivity type, formed in surface regions of said third semiconductor regions (13); a first electrode (23) electrically connected to said fourth semiconductor regions (14); a control electrode (21) disposed, via an insulating film (22), on the other principal surface between said first

semiconductor region (11) and said fourth semiconductor regions (14); and a second electrode (20) electrically connected to said second semiconductor regions (12), said method comprising:

a step of forming a fifth semiconductor region (15) having the first conductivity type in the one principal surface of said first semiconductor region (11) so as to be adjacent to said second semiconductor regions (12); and

a step of forming a sixth semiconductor region (16) having the second conductivity type, between said fifth semiconductor region (15) and said first semiconductor region (11).